LISTING OF CLAIMS

1. (Previously Presented) A method, comprising:

monitoring a state of a multi-threaded application running in a system and a buffer associated with the multi-threaded application, wherein each thread includes one or more activities to be executed by the system;

determining availability of a processor to perform simultaneous multi-threading and the buffer;

coordinating dispatch of threads of the multi-threaded application to increase execution overlap of activities executing in the system based, at least in part, on the availability of the buffer;

dynamically adjusting one or more of the frequency or the voltage applied to the processor based, at least in part, on the availability of the buffer and the coordination of the dispatch of the threads; and

dynamically adjusting the buffer size based, at least in part, on the adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads.

2. (Previously Presented) The method of claim 1, wherein coordinating dispatch of the threads of the multi-threaded application includes assessing execution readiness of the one or more activities of each thread.

3. (Previously Presented) The method of claim 2, wherein coordinating dispatch of the threads of the multi-threaded application includes delaying a ready-to-be-dispatched activity from being dispatched.

4. (Previously Presented) The method of claim 3, wherein a first activity is delayed from being dispatched to wait for a second activity to be ready so that both the first and second activities are dispatched together, and wherein the first and second activities are from one or more applications.

5-6. (Cancelled).

7. (Previously Presented) The method of claim 1, further comprising

determining the availability of configurable hardware components including an arithmetic logic unit (ALU), and registers in the system, wherein coordinating dispatch of the threads of the multi-threaded application is further based on the availability of the configurable hardware components.

8-9. (Cancelled)

10. (Previously Presented) The method of claim 7, wherein adjusting the voltage applied to the processor includes powering on or powering off at least a portion of circuitry in the system.

11. (Previously Presented) The method of claim 1, wherein monitoring the buffer associated with the multi-threaded application includes monitoring buffer fullness levels of the buffer.

12. (Currently Amended) The method of claim 11, wherein monitoring the buffer fullness levels includes comparing ~~the~~ **a** buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark.

13. (Previously Presented) The method of claim 12, wherein comparing the buffer level includes determining buffer overflow and buffer underflow conditions based, at least in part, on the high level mark and the low level mark.

14. (Previously Presented) A computer readable storage medium containing executable instructions which, when executed in a processing system, causes the processing system to perform a method comprising:

monitoring a state of a multi-threaded application running in a system and a buffer associated with the multi-threaded application, wherein each thread includes one or more activities to be executed by the system;

determining availability of a processor to perform simultaneous multi-threading and the buffer;

coordinating dispatch of threads of the multi-threaded application to increase execution overlap of activities executing in the system based, at least in part, on the availability of the buffer;

dynamically adjusting one or more of the frequency or the voltage applied to the processor based, at least in part, on the availability of the buffer and the coordination of the dispatch of the threads; and

dynamically adjusting the buffer size based, at least in part, on the adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads.

15. (Previously Presented) The computer readable storage medium of claim 14, wherein coordinating dispatch of the threads of the multi-threaded application includes delaying a ready-to-be-dispatched activity from being dispatched.

16-18. (Cancelled)

19. (Currently Amended) The computer readable storage medium of claim 14,

wherein monitoring the buffer associated with the multi-threaded application includes monitoring buffer fullness levels of the buffer, and wherein monitoring the buffer fullness levels includes comparing ~~the~~ **a** buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark.

20-38. (Cancelled)

39. (Currently Amended) A system, comprising:

a memory to store data and instructions;

a processor coupled to said memory on a bus, said processor operable to perform instructions, said processor to include a bus unit to receive a sequence of instructions from said memory;

an execution unit coupled to said bus unit, said execution unit to execute said sequence of

instructions, said sequence of instructions to cause said execution unit to:

monitor a state of a multi-threaded application running [[in]] **and** a system buffer associated with the multi-threaded application, wherein each thread includes one or more activities to be executed by the system;

determine availability of a processor to perform simultaneous multi-threading and the **system** buffer;

coordinate dispatch of threads of the multi-threaded application to increase execution overlap of activities executing in the system based, at least in part, on the availability of the **system** buffer;

dynamically adjust one or more of the frequency or the voltage applied to the processor based, at least in part, on the availability of the **system** buffer and the coordination of the dispatch of the threads; and

dynamically adjust the **system** buffer size based, at least in part, on the adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads.

40. (Previously Presented) The system of claim 39, wherein said coordinating dispatch of the threads of the multi-threaded application includes delaying a ready-to-be-dispatched activity from being dispatched.

41-50. (Cancelled)